Sephy

H2020 Programme
Space Theme

SEPHY DATASHEET

SEPHY
Grant No. 640243

Deliverable Information

Work Package	4	**Dissemination Level of Deliverable[1]:**		CO
Deliverable Number	D4.2			
Date of Issue	28/04/2017			
Document Reference	D4.2 SEPHY DATASHEET			
Version Number	1			
Nature of Deliverable[2]	R☒	P☐	D☐	O☐
Keywords	Guidelines, Rules, Recommendations			

Abstract

This document contains a description of the SEPHY chip, its basic functionality, pinout and modes.

[1] Dissemination level: **PU** = Public; **PP** = Restricted to other programme participants (including the Commission Services); **RE** = Restricted to a group specified by the consortium (including the Commission Services); **CO** = Confidential, only for members of the consortium (including the Commission Services).
[2] Nature of deliverable: **R** = Report; **P** = Prototype; **D** = Demonstrator; **O** = Other

Document Authors

ENTITY	CONTRIBUTORS
ARQ	López, Jesús Gutierro, Úrsula
IHP	Krstic, Milos

Document Change Record

ISSUE	DATE	CHANGE PROPOSAL Nº	AFFECTED PARAGRAPHS	DESCRIPCIÓN DEL CAMBIO CHANGE DESCRIPTION
Issue 1	27/04/2017	1	All	Creation

Disclosure Statement

Table of Contents

List of Tables

List of Figures

List of Acronyms

ACRONYM	MEANING
AAF	Anti Aliasing Filter
ADC	Analog to Digital Converter
ASIC	Application-Specific Integrated Circuit
CDM	Charged Device Model
DAC	Digital to Analog Converter
DRV	Driver
ENOB	Effective Number Of Bits
ESD	Electro Static Discharge
GMII	Gigabit Media Independent Interface
HBM	Human Body Model
LET	Liner Energy Transfer
MDC	Management Data Clock
MDIO	Management Data I/O
MII	Media Independent Interface
MM	Machine Model
PD	Phase Detector
PGA	Programmable Gain Amplifier
PLL	Phase Lock Loop
PTAT	Proportional To Absolute Temperature
RHA	Radhard
RMII	Reduced Media Independent Interface
RH	Radiation Hardened
SEPHY	Space Ethernet PHY
SEL	Single Event Latch-up

SEU	Single Event Upset
TC	Test Chip
TID	Total Ionizing Dose
TMI	Test Management Interface
VCO	Voltage Controlled Oscillator

Table 0-1 – List of acronyms.

Executive Summary

This document contains a description of the SEPHY chip, its basic functionality, pinout and modes for the final user.

SEPHY
RADIATION HARDENED SINGLE PORT 10/100 MB/S ETHERNET PHYSICAL LAYER TRANSCEIVER

OVERVIEW

SEPHY is a Physical Layer device for Ethernet 10BASE-T and 100BASE-TX using category 5 Unshielded, Type 1 Shielded cables suitable for use in harsh and radiation environments. It integrates all the physical-layer functions needed to transmit and receive data. This device supports the standard and reduced Media Independent Interface (MII/RMII) for direct connection to a Media Access Controller (MAC)

SEPHY uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT 5 twisted-pair wiring.

FEATURES

- IEEE 802.3 10BASE-T compatible
- IEEE 802.3 100BASE-TX compatible
- ANSI X3.263-1995 compatible
- Integrated high performance 100 Mb/s clock recovery circuitry requiring no external filters
- Full Duplex support for 10 and 100 Mb/s
- Programmable loopback modes for easy system diagnostics
- 3.3V/1.8V power supply.
- Extended temperature range from -55°C to 125°C
- Cold spare functionality.
- MII/RMII MAC communication interface
- MI interface for MAC management and diagnostics
- 15 years lifetime at maximum operating conditions
- TID greater than 100krad
- SEU threshold LET 30MeV/mg/cm²
- SEU Error Rate lower than 10^{-10} errors/bit-day (@ <70 MeV/mg/cm²)
- SEL Threshold LET greater than 60 MeV/mg/cm²
- QFP64 package

1 SYSTEM DIAGRAM

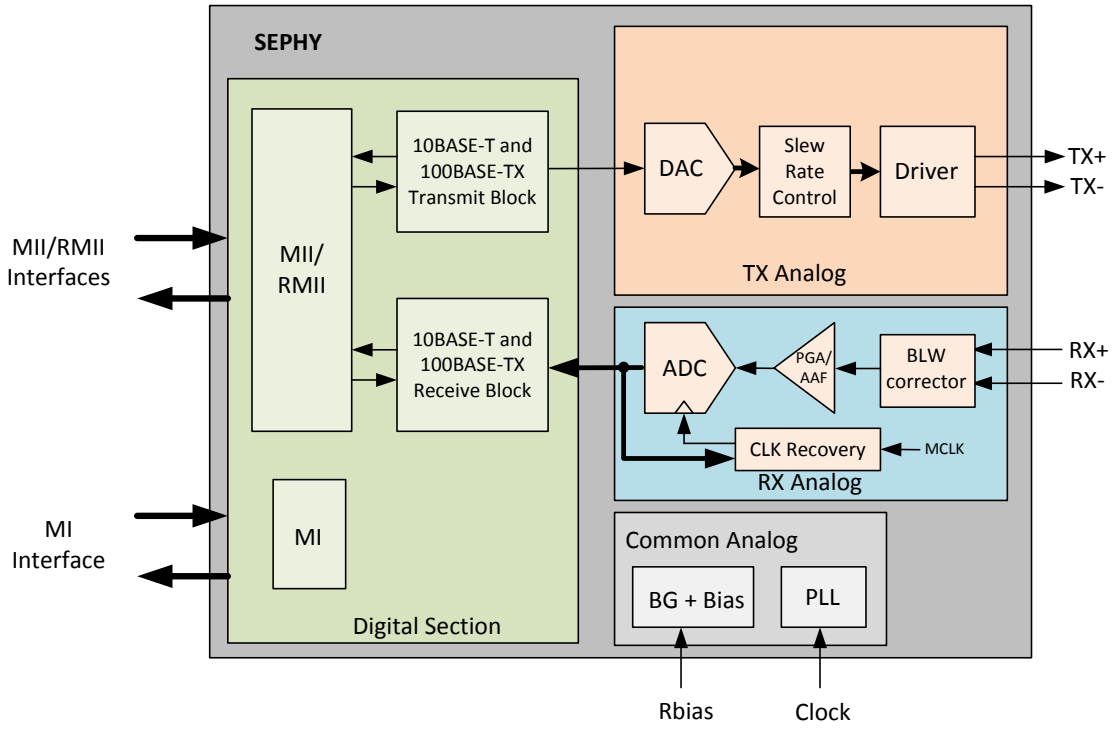


Figure 1-1: SEPHY system diagram

2 RADIATION HARDENING

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	-	100	300	Krad	
SEL	60	-	-	MeVcm^2/mg	
SEU/SET	30	-	-	MeVcm^2/mg	
SEU/SET	-	70	-	MeVcm^2/mg	BER=10^{-10}

3 AVAILABLE OPTIONS

PRODUCT	Quality Level	PACKAGE	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA
SEPHY-S	S - Space	TBD	-55^{o}C to 125^{o}C	TBD	250-piece tray (TBC)
SEPHY-I	I - Industrial	TBD	TBD	TBD	250-piece tray (TBC)

4 PIN DIAGRAM

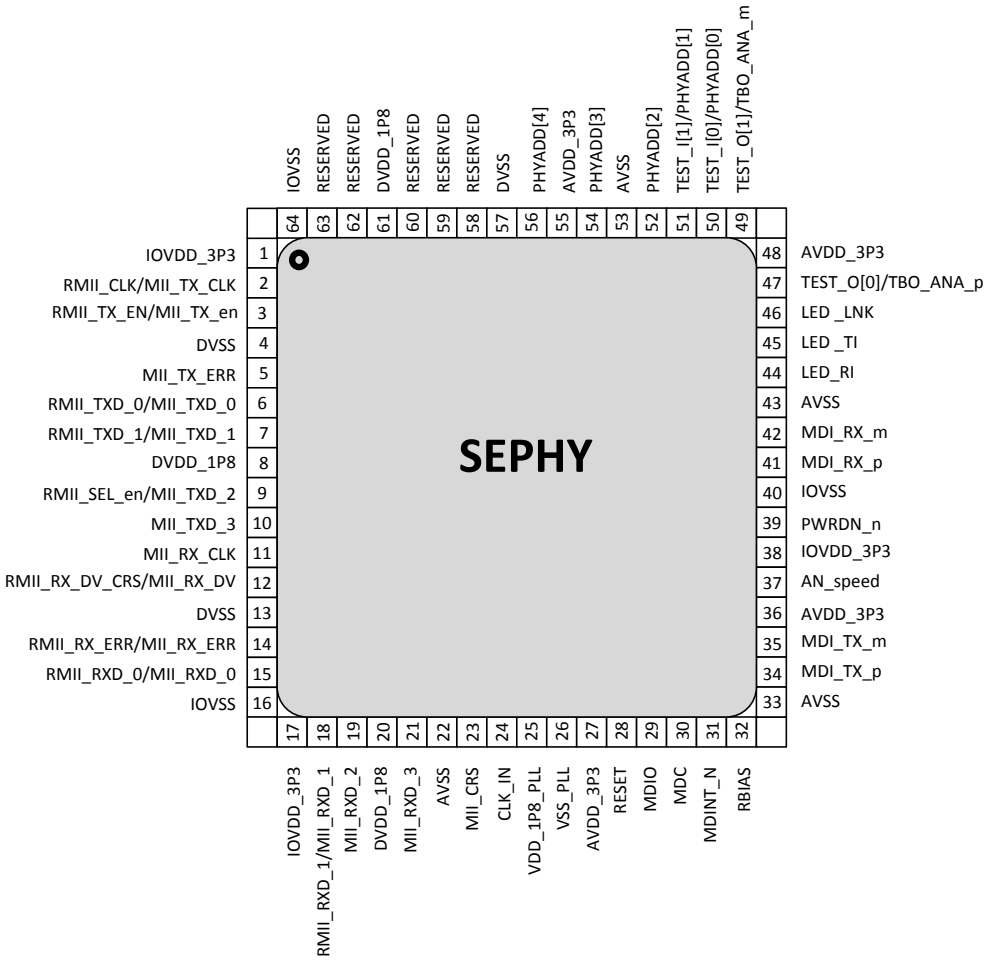


Figure 4-1: SEPHY pinout

5 ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Maximum rating	Units
I/O Supply Voltage	AVDD_3P3	-0.5 to 3.6 (TBC)	V
Core Supply Voltage	DVDD_1P8	-0.5 to 2	V
PLL Supply Voltage	VDD_PLL_1P8	-0.5 to 2	V
I/O pins	N/A	-0.5 to 3.6	V
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Junction Temperature	T_J	-55 to 150	°C
Soldering lead temperature (10 s)	T_{SOL}	300	°C
ESD	V_{HBM} V_{CDM} V_{MM}	2000 250 >100	V

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Nom	Max	Units
I/O Supply Voltage	AVDD_3P3	3	3.3	3.6	V
Core Supply Voltage	DVDD_1P8	1.62	1.8	1.98	V
PLL Supply Voltage	VDD_PLL_1P8	1.62	1.8	1.98	V
Input High Voltage (LVTTL&LVCMOS)	V_{IH}	2		3.6	V
Input Low Voltage (LVTTL&LVCMOS)	V_{IL}	0		0.8	V
Output High Voltage (LVTTL)	V_{OH}	2.4			V
Output Low Voltage (LVTTL)	V_{OL}	0		0.4	V

Table 5-1: Recommended Operating Conditions

5.3 DC SPECIFICATIONS

5.3.1 Electrical Characteristics

Parameter		Min	Nom	Max	Units
V_{IH}	Input High Voltage	2			V
V_{IL}	Input Low Voltage			0.8	V
I_{IH}	Input High Current				µA
I_{IL}	Input Low Current				µA
V_{OH}	Output Low Voltage	2.4			V
V_{OL}	Output Low Voltage			0.4	V
I_{OZ}	Tri-State Leakage			10	µA
I_{CS}	Cold Spare Leakage			10	µA
I_{dd100}	100BASE-TX			TBD	mA
I_{dd10}	10BASE-T			TBD	mA
I_{PD}	Power Down Mode			TBD	mA

6 FUNCTIONAL DESCRIPTION

SEPHY 10/100 Mb/s Ethernet Physical Layer integrates a 100BASE-TX Physical Coding Sub-layer (PCS) and a complete 10BASE-T module in a single chip. It provides a standard Media Independent Interface (MII) and reduced Independent Interface (RMII) to communicate between the Physical Signalling and the Medium Access Control (MAC) layers for both 100BASE-TX and 10BASE-T operations. It has a Management interface (MI) in order to access the configuration registers.

The 10BASE-T section of the device consists of the transmitter and receiver blocks.

- Transmitter
  - MAU transmit functions
  - Jabber
  - Manchester encoder
  - Wave-shaping FIR
  - 10BASE-T Driver
- Receiver
  - MAU receive functions
  - Manchester decoder
  - 10BASE-T clock recovery
  - Reception FSM

The 100BASE-TX section of the device consists of the following functional blocks:

- Transmitter
  - 4B/5B Encoder
  - NRZ Encoder
  - Scrambler
  - MLT3 encoder
  - 100BASE-TX Driver
- Receiver
  - 4B/5B Encoder
  - NRZ Encoder
  - Scrambler
  - MLT3 encoder
  - Baseline Wander Correction
  - Clock recovery module
  - Programmable Gain Amplifier

The 100BASE-TX and 10BASE-T sections share the following functional blocks:

- TX DAC
- RX ADC
- MII status/control registers
- MI interface

6.1 MII Interface

SEPHY incorporates the media independent interface (MII) as specified in Clause 22 of the IEEE802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. The MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC). TX and RX clocks should run at 25MHz.

6.2 RMII Interface

SEPHY incorporates the reduced media independent interface (RMII) to reduce the number of pins in relation to MII, as specified in the RMII specification (rev1.2) from the RMII Consortium. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. The RMII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC). RMII clock should run at 50MHz.

6.3 MI Interface

The MI specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO. SEPHY implements all the required MI registers as well as several optional registers. A description of the serial management access protocol follows.

6.3.1 MI Access Protocol

The MI interface consists of two pins, management data clock (MDC) and management data input/output (MDIO). MDC has a maximum clock rate of 25 MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices with unique PHYADD. The MDIO frame format is shown below in Table 6-1.

The MDIO pin requires a pull-up resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide SEPHY with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles. In addition 32 MDC clock cycles should be used to re-sync the device if an invalid start, opcode, or turnaround bit is detected.

SEPHY waits until it has received this preamble sequence before responding to any other transaction. Once SEPHY MI port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid start, invalid opcode, or invalid turnaround bit has occurred.

The start code (ST) is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state. The operation code (OP) for a read transaction is <10>, while the operation code for a write transaction is <01>. Turnaround (TA) is defined as an idle bit time inserted between the register address field and the data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of turnaround. The addressed SEPHY drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station management entity writes data to the addressed SEPHY thus eliminating the requirement for MDIO turnaround. The turnaround time is filled by the management entity by inserting <10>. Figure 6-1 shows the relationship between MDC and the MDIO as driven or received by the station (STA) and SEPHY (PHY) for a typical register write/read access.

The IDLE condition on MDIO is a high-impedance state. All three state drivers are disabled and the SEPHY's pull-up resistor will pull the MDIO line to a logic one.

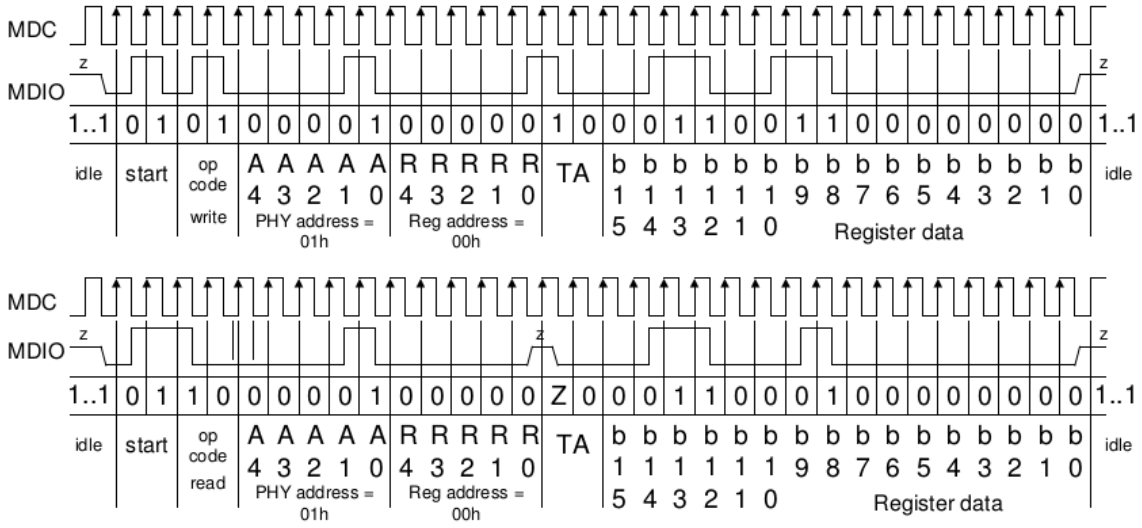


Figure 6-1 MI Interface Write/Read Operations

Command	Preamble [31:0]	ST [1:0]	OP [1:0]	PHYADD [4:0]	REAGADD [4:0]	TA [1:0]	DATA [15:0]	IDLE [0]
Read	11…1	01	10	aaaaa	RRRRR	Z0	DD…D	Z
Write	11…1	01	01	aaaaa	RRRRR	10	DD…D	Z

Table 6-1 MI Interface Protocol

7 ARCHITECTURE

7.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII/RMII, to a scrambled MLT-3 125 Mb/s serial data stream. Because the 100BASE-TX TP-PMD is integrated, the differential output pins, PMD output pair, can be directly routed to the magnetics.

The block diagram in provides an overview of each functional block within the 100BASE-TX transmit section.

The transmitter section consists of the following functional blocks:

- Code-group encoder and injection block
- Scrambler block (bypass option)
- NRZ to NRZI encoder block
- Binary to MLT-3 converter or common driver

SEPHY implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

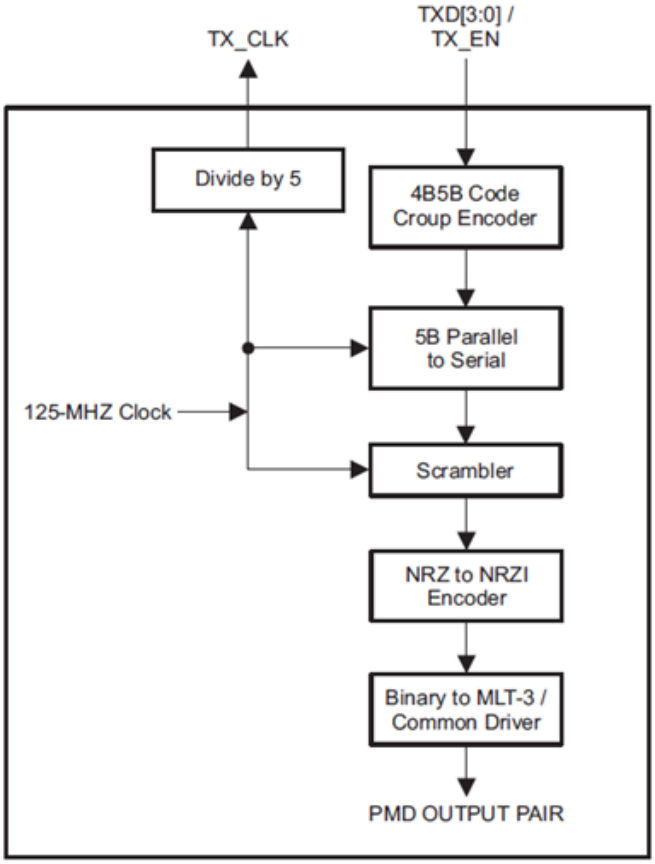


Figure 7-1 100BASE-TX Block Diagram

7.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII/RMII. Because the 100BASE-TX TP-PMD is integrated, the differential input pins, RD±, can be directly routed from the AC coupling magnetics.
See Figure 7-2 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.
The receive section consists of the following functional blocks:

- Analog front end
- Digital signal processor
- Signal detect
- MLT-3 to binary decoder
- NRZI to NRZ decoder
- Serial to parallel
- Descrambler
- Code group alignment
- 4B/5B decoder
- Link integrity monitor
- Data Valid detection

7.2.1 Analog Front End

In addition to the digital equalization and gain control, SEPHY includes gain and BLW correction in the analog front end.

7.2.2 Digital Signal Processor

The digital signal processor includes adaptive equalization with gain control, clock recovery and base line wander correction.

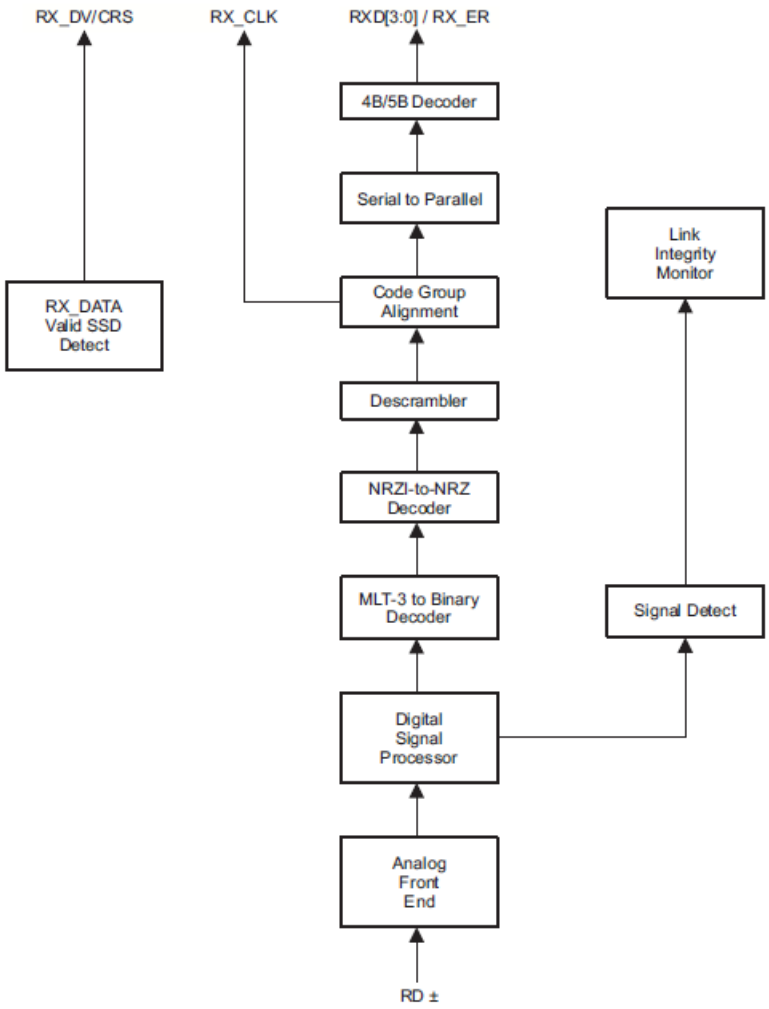


Figure 7-2 100BASE-TX Receive Block Diagram

7.2.3 Digital Adaptive Equalization and Gain Control

When transmitting data at high speeds over copper twisted pair cable, frequency dependent attenuation becomes a concern. In high-speed twisted pair signalling, the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated to ensure the integrity of the transmission.

In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation which will overcompensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. The compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

SEPHY utilizes an extremely robust equalization scheme referred as ‘digital adaptive equalization’.

The digital equalizer removes inter symbol interference (ISI) from the receive data stream by continuously adapting to provide a filter with the inverse frequency response of the channel. Equalization is combined with an adaptive gain control stage. This enables the receive 'eye pattern' to be opened sufficiently to allow very reliable data recovery.

The curves given in Figure 7-3 illustrate attenuation at certain frequencies for given cable lengths. This is derived from the worst case frequency vs. attenuation figures as specified in the EIA/TIA Bulletin TSB-36.
These curves indicate the significant variations in signal attenuation that must be compensated for by the receive adaptive equalization circuit.

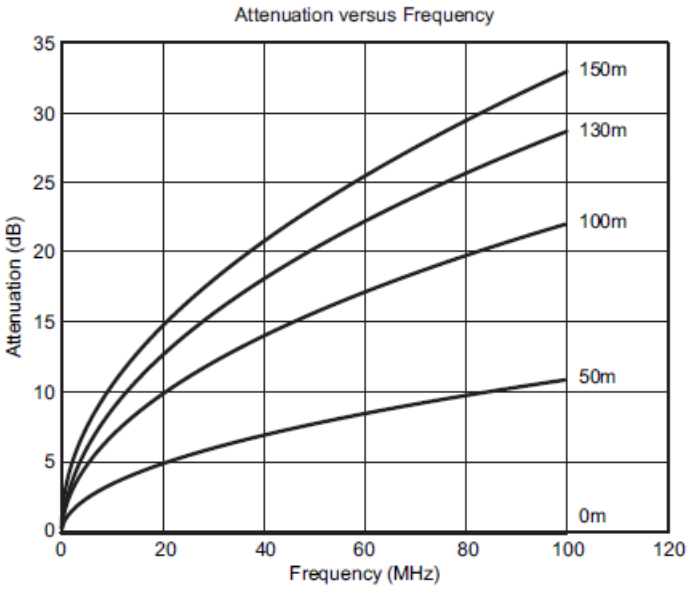


Figure 7-3 EIA/TIA Attenuation vs. Frequency for 0, 50, 100, 130 and 150 meters of CAT 5 cable

SEPHY is completely ANSI TP-PMD compliant and includes base line wander (BLW) compensation. The BLW compensation block can successfully recover the TPPMD defined “killer” pattern. BLW can generally be defined as the change in the average DC content, relatively short period over time, of an AC coupled digital transmission over a given transmission medium. (i.e., copper wire). BLW results from the interaction between the low frequency components of a transmitted bit stream and the frequency response of the AC coupling components within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformers then the droop characteristics of the transformers will dominate resulting in potentially serious BLW.

This event can be as large as 800 mV of DC offset for a period of 120 µs. If left uncompensated, events such as this can cause packet loss.

7.3 10BASE-T Transceiver

The 10BASE-T transceiver module is IEEE 802.3 compliant. It includes the receiver, transmitter, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard. It includes a digital FIR filter in order to shape the output signal to meet the TX template specified in the standard. An external filter is not required on the 10BASE-T interface since this is integrated inside the SEPHY. This section focuses on the general 10BASET system level operation.

7.3.1 Normal Link Pulse Detection/Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-T standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

If valid link pulses are not received, the link detector disables the 10BASE-T twisted pair transmitter, receiver and collision detection functions.

7.3.2 Jabber Function

The jabber function monitors the SEPHY's output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active.

7.3.3 Transmit and Receive Filtering

External 10BASE-T filters are not required when using SEPHY, as the required signal conditioning is integrated into the device. Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

7.3.4 Transmitter

The encoder begins operation when the transmit enable input (TX_EN) goes high and converts NRZ data to preemphasized Manchester data for the transceiver. For the duration of TX_EN, the serialized transmit data (TXD) is encoded for the transmit-driver pair (PMD Output Pair). TXD must be valid on the rising edge of transmit clock (TX_CLK). Transmission ends when TX_EN deasserts. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

7.3.5 Receiver

The decoder detects the end of a frame when no additional mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

8 CONFIGURATION

8.1 SPEED Pin Control

The SEPHY speed mode can be controlled unsign the external pin named AN_SPEED. If set to LOW during power up or reset will set 10BASE-T mode. If set to HIGH will set 100BASE-TX mode. The pin value at power up or reset will be stored at the Control Register (CTRL) at bit SPEEDSEL. This can be also modified via MI interface.

8.2 PHY Address

The five PHY address inputs are mapped to the pins 50,51,52,54 and 56. PHYADD[1:0] are shared with TEST_I[1:0] signals and the PHYADD[1:0] values are set through the values in those pin at power up or reset.

8.3 LED Interface

SEPHY supports three light emitting diode (LED) pins, signalling LINK stablished, RX activity and TX activity.

8.4 Internal Loopback

SEPHY includes loopback test mode for facilitating systems diagnosis. The loopback mode is selected through bit 0.14 (LOOPBACK) of the CTRL register. Writing 1 to this bit enables MII

transmit data from TX± pins to be routed to the RX± pins. While in Loopback mode the data will not be received from the channel while transmission is kept.

8.5 Power Down

SEPHY supports power down mode which is activated forcing LOW at PWRDN_N pin (39). This mode switches down most of the internal circuitry and reduces power consumption to a minimum.

8.6 Clock Input

SEPHY uses an external clock at 25MHz, which should be provided through the CLK_IN pin (24).

8.7 MII/RMII interface

SEPHY includes two different MAC interfaces which can be used MII and RMII. In order to select between them, the RMII_SEL_EN pin (9) can be set to HIGH at power up or reset. This can be also performed through bit 19.14 (RMIIEN) of the CTRL1 register.

8.8 RESET OPERATION

SEPHY operation needs hardware reset after power on to ensure proper functionality. The reset it is synchronized with the LOCK signal provided by the PLL to ensure that reset is deasserted only if a stable clock from the PLL is provided.

If required during normal operation, the device can be reset by a hardware or software reset.

8.8.1 Hardware Reset

A hardware reset is accomplished by applying a high pulse (LVTTL level), with a duration of at least 1 µs, to the RESET pin (28). This will reset the device such that all registers will be reinitialized to default values and the hardware configuration values will be re-latched into the device (similar to the power-up/reset operation).

8.8.2 Software Reset

A software reset is accomplished by setting the reset bit (bit 0.15) of the Control register (CTRL). The software reset will reset the device such that all registers will be reset to default values and the hardware configuration values will be maintained. Software driver code must wait TBD following a software reset before allowing further serial MII/RMII operations with SEPHY.

9 MI management Registers

The MI basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII shall incorporate the basic register set.

Those PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). Registers 2 through 14 are part of the extended register set. SEPHY device do not to provide GMII, but the registers are showing here for convenience.

Register addresses 16 through 31 may be used to provide vendor-specific functions or abilities. In SEPHY, register address 31 provides access to test management interface registers

TMI registers set consists in 30 registers for test/manufacturer use only.

The device includes a MI interface in order to provide access to MII and TMI registers. The MI interface is described in 6.3.

MII registers definition

Register address	Register address (HEX)	Used/Not Used	TAG	Register name	Basic/Extended		
					MII	GMII	
0	0x00	Used	CTRL	Control	B	B	The **MII** basic register set consists of two registers referred to as the **Control register (Register 0)** and the **Status register (Register 1)**. All PHYs that provide an MII shall incorporate the basic register set.
1	0x01	Used	STS	Status	B	B	
2,3	0x02-0x03	Not Used	PHYID	PHY Identifier	E	E	All PHYs that provide a **GMII** shall incorporate an extended basic register set consisting of the **Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15)**. The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set. The format of Registers 4 through 10 is defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.
4	0x04	Not Used	ANA	Auto-Negotiation Advertisement	E	E	
5	0x05	Not Used	ANLPBPA	Auto-Negotiation Link Partner Base Page Ability	E	E	
6	0x06	Not Used	ANEXP	Auto-Negotiation Expansion	E	E	
7	0x07	Not Used	ANNPT	Auto-Negotiation Next Page Transmit	E	E	
8	0x08	Not Used	ANLPRNP	Auto-Negotiation Link Partner Received Next Page	E	E	
9	0x09	Not Used	MSCTRL	MASTER-SLAVE Control Register	E	E	

10	0x0A	Not Used	MSSTS	MASTER-SLAVE Status Register	E	E	
11	0x0B	Not Used	PSECTRL	PSE Control register	E	E	
12	0x0C	Not Used	PSESTS	PSE Status register	E	E	
13	0x0D	Not Used	MMDCTRL	MMD Access Control Register	E	E	
14	0x0E	Not Used	MMDADD	MMD Access Address Data Register	E	E	
15	0x0F	Not Used	EXSTS	Extended Status	Reserved	B	
16	0x10	Used	TXCFG	TX config	E	E	Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities.
17	0x11	Used	RXCFG	RX config	E	E	
18	0x12	Used	TESTCFG	Test config	E	E	
19	0x13	Used	CTRL1	Control 1	E	E	
20	0x14	Used	STATUS1	Status 1	E	E	
21	0x15	Used	EDACERR	EDAC corrected errors	E	E	
22	0x16	Used	EDACNERR	EDAC non-corrected errors	E	E	
23 through 30	0x17-0x1E	Not Used	N/A	Vendor Specific	E	E	
31	RESERVED	RESERVED	RESERVED	RESERVED	-	-	

B=BASIC E=EXTENDED

Register Bit Acronyms

Register address	Register address (HEX)	TAG	Register name	BIT															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0x00	CTRL	Control	RESET	LOOPBACK	SPEEDSELL	AUTONEGEN	POWERDWN	ISOLATE	RAUTONEGGEN	DM	CT	SPEEDSELM	UNIDIREN	N/A	N/A	N/A	N/A	N/A
1	0x01	STS	Status	100BASET4EN	100BASETXFDEN	100BASEXHFEN	10BASETFDEN	10BASETHDEN	100BASET2FDEN	100BASET2HDEN	EXTSTAT	UNIABI	MFPREAMSUP	AUTONEGCOM	REMFAULT	AUTONEGAB	LINKSTAT	JABDET	EXTCAP
2	0x02	PHYID0	PHY Identifier	PHYID<18>	PHYID<17>	PHYID<16>	PHYID<15>	PHYID<14>	PHYID<13>	PHYID<12>	PHYID<11>	PHYID<10>	PHYID<9>	PHYID<8>	PHYID<7>	PHYID<6>	PHYID<5>	PHYID<4>	PHYID<3>
3	0x03	PHYID1	PHY Identifier	PHYID<24>	PHYID<23>	PHYID<22>	PHYID<21>	PHYID<20>	PHYID<19>	MODNUM<5>	MODNUM<4>	MODNUM<3>	MODNUM<2>	MODNUM<1>	MODNUM<0>	REVNUM<3>	REVNUM<2>	REVNUM<1>	REVNUM<0>
16	0x10	TXCFG	TX config	PREAMGENEN	JABDIS	TXDIS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

17	0x11	RXCFG	RX config	RXDIS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
18	0x12	TESTCFG	Test config	TESTO<1>	TESTO<0>	TESTI<1>	TESTI<0>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
19	0x13	CTRL1	Control 1	MDIXEN	RMIIEN	EEEEN	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
20	0x14	STATUS1	Status 1	DESCRLCK	LEDTI	LEDRI	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
21	0x15	EDACERR	EDAC corrected errors	EDACCE<15>	EDACCE<14>	EDACCE<13>	EDACCE<12>	EDACCE<11>	EDACCE<10>	EDACCE<9>	EDACCE<8>	EDACCE<7>	EDACCE<6>	EDACCE<5>	EDACCE<4>	EDACCE<3>	EDACCE<2>	EDACCE<1>	EDACCE<0>
22	0x16	EDACNERR	EDAC non-corrected errors	EDACNCE<15>	EDACNCE<14>	EDACNCE<13>	EDACNCE<12>	EDACNCE<11>	EDACNCE<10>	EDACNCE<9>	EDACNCE<8>	EDACNCE<7>	EDACNCE<6>	EDACNCE<5>	EDACNCE<4>	EDACNCE<3>	EDACNCE<2>	EDACNCE<1>	EDACNCE<0>
31	RESERVED	RESERVED	RESERVED	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

MII Registers Definition

Control Register (0x00)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
0.15	Reset	1 = PHY reset 0 = normal operation All PHY functions are disabled. At recovery from Reset the PHY does the following: - Initalizes Analog Circuitry - Initializes all digital logic and state machines - Read and latches PHYAD pins - Initilializes MII registers to their default values	R/W SC	0	Y	RESET
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W	0	Y	LOOPBACK
0.13	Speed Selection (LSB)(1)	1 = 100 Mb/s 0 = 10 Mb/s	R/W	AN_speed	Y	SPEEDSELL
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	RO	0	N	AUTONEGEN
0.11	Power Down	1 = power down 0 = normal operation** Powers Down all functions but the serial management interface and clock circuitry. MII registers can be read/written. - Initializes all digital logic and state machines - MII registers are not reset to default - PHYAD pins are not re-read	R/W	0	Y	POWERDWN
0.10	Isolate	1 = electrically Isolate PHY from MII or OMIT 0 = normal operation**	R/W	0	Y	ISOLATE
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	RO	0	N	RAUTONEGGEN
0.8	Duplex Mode	1 = full duplex 0 = half duplex	RO	1	N	DM
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	RO	0	N	CT
0.6	Speed Selection (MSB)	Reserved	RO	0	N	SPEEDSELM
0.5	Unidirectional enable	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established	R/W	0	Y	UNIDIREN
0.4:0	Reserved for future standardization	Write as 0, ignore on read	RO	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high, SC=Self Clear

(1) The default value it is set by the value of AN_SPEED pin after reset.

Status Register (0x01)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0	Y	100BASET4EN
1.14	100BASE-TX Full Duplex	1 = PHY able to perform full duplex 100BASE-TX 0 = PHY not able to perform full duplex 100BASE-TX	RO	1	Y	100BASETXFDEN
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO	0	Y	100BASEXHFEN
1.12	10BASE-T Full Duplex	1 = PHY able to operate at 10BASE-T in full duplex mode 0 = PHY not able to operate at 10BASE-T in full duplex mode	RO	1	Y	10BASETFDEN
1.11	10BASE-T Half Duplex	1 = PHY able to operate at 10BASE-T in half duplex mode 0 = PHY not able to operate at 10BASE-T in half duplex mode	RO	0	Y	10BASETHDEN
1.10	100BASE-T2 Full Duplex	1= PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO	0	Y	100BASET2FDEN
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO	0	Y	100BASET2HDEN
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO	0	Y	EXTSTAT
1.7	Unidirectional ability	1= PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established	RO	1	Y	UNIABI
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed. 0 = PHY will not accept management frames with preamble suppressed.	RO	1	Y	MFPREAMSUP
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO	0	Y	AUTONEGCOM
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH	0	Y	REMFAULT
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	0	Y	AUTONEGAB
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL	0	Y	LINKSTAT
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH	0	Y	JABDET
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO	0	Y	EXTCAP

*R0 = Read only, LL = Latching low, LH = Latching high, SC=Self Clear

PHY Identifier Register 1 (0x02)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
2.15	PHY Identifier Bits (18:3)	Organizationally Unique Identifier (OUI), Bits 18:3	RO	TBD	Y	PHYID<18>
2.14						PHYID<17>
2.13						PHYID<16>
2.12						PHYID<15>
2.11						PHYID<14>
2.10						PHYID<13>
2.9						PHYID<12>
2.8						PHYID<11>
2.7						PHYID<10>
2.6						PHYID<9>
2.5						PHYID<8>
2.4						PHYID<7>
2.3						PHYID<6>
2.2						PHYID<5>
2.1						PHYID<4>
2.0						PHYID<3>

*R0 = Read only, LL = Latching low, LH = Latching high

PHY Identifier Register 1 (0x03)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
3.15	PHY Identifier Bits (24:19)	Organizationally Unique Identifier (OUI), Bits 24:19	RO	TBD	Y	PHYID<24>
3.14						PHYID<23>
3.13						PHYID<22>
3.12						PHYID<21>
3.11						PHYID<20>
3.10						PHYID<19>
3.9	Model Number	Model Number	RO	TBD	Y	MODNUM<5>
3.8						MODNUM<4>
3.7						MODNUM<3>
3.6						MODNUM<2>
3.5						MODNUM<1>
3.4						MODNUM<0>
3.3	Revision Number	Revision Number	RO	0	Y	REVNUM<3>
3.2						REVNUM<2>
3.1						REVNUM<1>
3.0						REVNUM<0>

*R0 = Read only, LL = Latching low, LH = Latching high

TX config (0x10)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
16.15	Preamble Generation Enable	1 = Enable preamble generation for 10BASE-T 0 = Disable preamble generation for 10BASE-T	RO	0	Y	PREAMGENEN
16.14	Jabber Disable (10BASE-T)	1 = Disable Jabber for 10BASE-T 0 = Enable Jabber for 10BASE-T	R/W	0	Y	JABDIS
16.13	TX_disable	1 = Disable Transmitter 0 = Enable Transmitter	R/W	0	Y	TXDIS
16.12	N/A	For Future Use	R/W	0	N	N/A
16.11	N/A	For Future Use	R/W	0	N	N/A
16.10	N/A	For Future Use	R/W	0	N	N/A
16.9	N/A	For Future Use	R/W	0	N	N/A
16.8	N/A	For Future Use	R/W	0	N	N/A
16.7	N/A	For Future Use	R/W	0	N	N/A
16.6	N/A	For Future Use	R/W	0	N	N/A
16.5	N/A	For Future Use	R/W	0	N	N/A
16.4	N/A	For Future Use	R/W	0	N	N/A
16.3	N/A	For Future Use	R/W	0	N	N/A
16.2	N/A	For Future Use	R/W	0	N	N/A
16.1	N/A	For Future Use	R/W	0	N	N/A
16.0	N/A	For Future Use	R/W	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high

RX config (0x11)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
17.15	RX disable	1 = Disable Receiver 0 = Enable Receiver	R/W	0	Y	RXDIS
17.14	N/A	For Future Use	R/W	0	Y	N/A
17.13	N/A	For Future Use	R/W	0	Y	N/A
17.12	N/A	For Future Use	R/W	0	N	N/A
17.11	N/A	For Future Use	R/W	0	N	N/A
17.10	N/A	For Future Use	R/W	0	N	N/A
17.9	N/A	For Future Use	R/W	0	N	N/A
17,8	N/A	For Future Use	R/W	0	N	N/A
17.7	N/A	For Future Use	R/W	0	N	N/A
17.6	N/A	For Future Use	R/W	0	N	N/A
17.5	N/A	For Future Use	R/W	0	N	N/A
17.4	N/A	For Future Use	R/W	0	N	N/A
17.3	N/A	For Future Use	R/W	0	N	N/A
17.2	N/A	For Future Use	R/W	0	N	N/A
17.1	N/A	For Future Use	R/W	0	N	N/A
17.0	N/A	For Future Use	R/W	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high

Test config (0x12)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
18.15	TEST_O<1:0>	1 = Set TEST_O<1> pin to '1' 0 = Set TEST_O<1> pin to '0'	R/W	0	Y	TESTO<1>
18.14		1 = Set TEST_O<0> pin to '1' 0 = Set TEST_O<0> pin to '0'	R/W	0	Y	TESTO<0>
18.13	TEST_I <1:0>	1 = TEST_I<1> pin is pulled to '1' externally 0 = TEST_I<1> pin is pulled to '0' externally	RO	0	Y	TESTI<1>
18.12		1 = TEST_I<0> pin is pulled to '1' externally 0 = TEST_I<0> pin is pulled to '0' externally	RO	0	Y	TESTI<0>
18.11	N/A	For Future Use	RO	0	N	N/A
18.10	N/A	For Future Use	RO	0	N	N/A
18.9	N/A	For Future Use	RO	0	N	N/A
18.8	N/A	For Future Use	RO	0	N	N/A
18.7	N/A	For Future Use	RO	0	N	N/A
18.6	N/A	For Future Use	RO	0	N	N/A
18.5	N/A	For Future Use	RO	0	N	N/A
18.4	N/A	For Future Use	RO	0	N	N/A
18.3	N/A	For Future Use	RO	0	N	N/A
18.2	N/A	For Future Use	RO	0	N	N/A
18.1	N/A	For Future Use	RO	0	N	N/A
18.0	N/A	For Future Use	RO	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high

Control 1 config (0x13)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
19.15	MDIX mode Enable	1 = Enable MDIX mode 0 = Disable MDIX mode	R/W	MDIX_en pin(1)	Y	MDIXEN
19.14	RMII Interface Enable	1 = Enable RMII interface 0 = Enable MII interface	R/W	RMII_SEL_en pin(2)	Y	RMIIEN
19.13	N/A	For Future Use	RO	0	N	N/A
19.12	N/A	For Future Use	RO	0	N	N/A
19.11	N/A	For Future Use	RO	0	N	N/A
19.10	N/A	For Future Use	RO	0	N	N/A
19.9	N/A	For Future Use	RO	0	N	N/A
19.8	N/A	For Future Use	RO	0	N	N/A
19.7	N/A	For Future Use	RO	0	N	N/A
19.6	N/A	For Future Use	RO	0	N	N/A
19.5	N/A	For Future Use	RO	0	N	N/A
19.4	N/A	For Future Use	RO	0	N	N/A
19.3	N/A	For Future Use	RO	0	N	N/A
19.2	N/A	For Future Use	RO	0	N	N/A
19.1	N/A	For Future Use	RO	0	N	N/A
19.0	N/A	For Future Use	RO	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high
(1) The default value it is set by the value of MDIX_en pin after reset.
(2) The default value it is set by the value of RMII_SEL_en pin after reset.

STATUS 1 (0x14)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
20.15	Descrambler Lock	1 = Descrambler Locked 0 = Descrambler Not Locked	RO	0	Y	DESCRLCK
20.14	LED _TI	1 = Transmission activity 0 = No Transmission activity	RO	0	Y	LEDTI
20.13	LED_RI	1 = Recepcion activity 0 = No Reception activity	RO	0	Y	LEDRI
20.12	N/A	For Future Use	RO	0	N	N/A
20.11	N/A	For Future Use	RO	0	N	N/A
20.10	N/A	For Future Use	RO	0	N	N/A
20.9	N/A	For Future Use	RO	0	N	N/A
20.8	N/A	For Future Use	RO	0	N	N/A
20.7	N/A	For Future Use	RO	0	N	N/A
20.6	N/A	For Future Use	RO	0	N	N/A
20.5	N/A	For Future Use	RO	0	N	N/A
20.4	N/A	For Future Use	RO	0	N	N/A
20.3	N/A	For Future Use	RO	0	N	N/A
20.2	N/A	For Future Use	RO	0	N	N/A
20.1	N/A	For Future Use	RO	0	N	N/A
20.0	N/A	For Future Use	RO	0	N	N/A

*R0 = Read only, LL = Latching low, LH = Latching high

EDAC CE (0x15)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
21.15	EDAC Corrected Errors Counter Bits (15:0)	Count of the EDAC Corrected Errors in configuration registers	RO	0	Y	EDACCE<15>
21.14				0	Y	EDACCE<14>
21.13				0	Y	EDACCE<13>
21.12				0	Y	EDACCE<12>
21.11				0	Y	EDACCE<11>
21.10				0	Y	EDACCE<10>
21.9				0	Y	EDACCE<9>
21.8				0	Y	EDACCE<8>
21.7				0	Y	EDACCE<7>
21.6				0	Y	EDACCE<6>
21.5				0	Y	EDACCE<5>
21.4				0	Y	EDACCE<4>
21.3				0	Y	EDACCE<3>
21.2				0	Y	EDACCE<2>
21.1				0	Y	EDACCE<1>
21.0				0	Y	EDACCE<0>

EDAC NCE (0x16)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
22.15	EDAC Non-Corrected Errors Counter Bits (15:0)	Count of the EDAC Non-Corrected Errors in registers	RO	0	Y	EDACNCE<15>
22.14				0	Y	EDACNCE<14>
22.13				0	Y	EDACNCE<13>
22.12				0	Y	EDACNCE<12>
22.11				0	Y	EDACNCE<11>
22.10				0	Y	EDACNCE<10>
22.9				0	Y	EDACNCE<9>
22.8				0	Y	EDACNCE<8>
22.7				0	Y	EDACNCE<7>
22.6				0	Y	EDACNCE<6>
22.5				0	Y	EDACNCE<5>
22.4				0	Y	EDACNCE<4>
22.3				0	Y	EDACNCE<3>
22.2				0	Y	EDACNCE<2>
22.1				0	Y	EDACNCE<1>
22.0				0	Y	EDACNCE<0>

Test MI register (0x1F)

Bit(s)	Name	Description	R/W*	Default	Used	Tag
31.15	TMI Registers Enable	1 = Access to TMI registers Enabled 0 = Access to TMI registers disabled	R/W	0	Y	TMIREGEN
31.14	N/A	For Future Use	N/A	N/A	N	N/A
31.13	N/A	For Future Use	N/A	N/A	N	N/A
31.12	N/A	For Future Use	N/A	N/A	N	N/A
31.11	N/A	For Future Use	N/A	N/A	N	N/A
31.10	N/A	For Future Use	N/A	N/A	N	N/A
31.9	N/A	For Future Use	N/A	N/A	N	N/A
31.8	N/A	For Future Use	N/A	N/A	N	N/A
31.7	N/A	For Future Use	N/A	N/A	N	N/A
31.6	N/A	For Future Use	N/A	N/A	N	N/A
31.5	N/A	For Future Use	N/A	N/A	N	N/A
31.4	N/A	For Future Use	N/A	N/A	N	N/A
31.3	N/A	For Future Use	N/A	N/A	N	N/A
31.2	N/A	For Future Use	N/A	N/A	N	N/A
31.1	N/A	For Future Use	N/A	N/A	N	N/A
31.0	N/A	For Future Use	N/A	N/A	N	N/A

10 PINOUT DESCRIPTION

Nº	Name	Type	Description
1	IOVDD_3P3	P	3.3V IO power supply
2	RMII_CLK/MII_TX_CLK	I/O	**RMII/MII TRANSMIT CLOCK**: provides the reference clock for the interface. If RMII is used, then this clock is configured as input and it will be used as transmit and receive clock. It should work at 50MHz. If MII is used, this clock will be configured as an output. The transmit clk frequency is 25MHz (100BASE-TX)/2.5MHz(10BASE-T)
3	RMII_TX_en/MII_TX_en	I	**RMII/MII TRANSMIT ENABLE**: is presented on the rising edge of the RMII_TX_CLK . It indicates the presence of valid data inputs on RMII/MII_TXD[3:0]. It is an active high signal.
4	DVSS	P	Core Ground
5	MII_TX_ERR	I	**MII TRANSMIT ERROR**: This signal can be used by a repeater to force the propagation of received errors.
6	RMII_TXD_0/MII_TXD_0	I	**RMII/MII TRANSMIT DATA:** The transmit data nibble received from the MAC that is synchronous to the rising edge of the RMII/MII_TX_CLK. If RMII is used, then the data will be transmitted through TXD[1:0]. If MII is used, then the data is codified in 4 bits TXD[3:0]
7	RMII_TXD_1/MII_TXD_1	I	**RMII/MII TRANSMIT DATA:** The transmit data nibble received from the MAC that is synchronous to the rising edge of the RMII/MII_TX_CLK. If RMII is used, then the data will be transmitted through TXD[1:0]. If MII is used,

			then the data is codified in 4 bits TXD[3:0]
8	DVDD_1P8	P	1.8V core power supply
9	RMII_SEL_en/MII_TXD_2	I	**MII TRANSMIT DATA:** The transmit data nibble received from the MAC that is synchronous to the rising edge of the RMII/MII_TX_CLK. If RMII is used, then the data will be transmitted through TXD[1:0]. If MII is used, then the data is codified in 4 bits TXD[3:0] **RMII_SEL_EN**: If MII_RXD_3/RMII_SEL_en pin is high during the falling edge of RESET pin, RMII interface is selected.
10	MII_TXD_3	I	**MII TRANSMIT DATA:** The transmit data nibble received from the MAC that is synchronous to the rising edge of the RMII/MII_TX_CLK. If RMII is used, then the data will be transmitted through TXD[1:0]. If MII is used, then the data is codified in 4 bits TXD[3:0]
11	MII_RX_CLK	O	**MII RECEIVE CLOCK**: When MII interface is used, this is the receive reference clock.
12	RMII_RX_DV_CRS/MII_RX_DV	O	**RMII RECEIVE DATA VALID & CARRIER SENSE/MII RECEIVE DATA VALID** This pin indicates valid data is present on the corresponding RXD[3:0].
13	DVSS	P	Core Ground
14	RMII_RX_ERR/MII_RX_ERR	O	**RMII/MII RECEIVE ERROR**: This pin indicates that an error symbol has been detected within a received packet.
15	RMII_RXD_0/MII_RXD_0	O	**RMII/MII RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to MII_RX_CLK. They contain valid

			data when MII_RX_DV is asserted. If RMII is used, then the data will be received through RXD[1:0] If MII is used, then the data is codified through RXD[3:0].
16	IOVSS	P	IO Ground
17	IOVDD_3P3	P	3.3V IO power supply
18	RMII_RXD_1/MII_RXD_1	O	**RMII/MII RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to MII_RX_CLK. They contain valid data when MII_RX_DV is asserted. If RMII is used, then the data will be received through RXD[1:0] If MII is used, then the data is codified through RXD[3:0].
19	MII_RXD_2	O	**MII RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to MII_RX_CLK. They contain valid data when MII_RX_DV is asserted.
20	DVDD_1P8	P	1.8V core power supply
21	MII_RXD_3	O	**MII RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to MII_RX_CLK. They contain valid data when MII_RX_DV is asserted. If MII is used, then the data is codified through RXD[3:0]
22	AVSS	P	Analog Ground
23	MII_CRS	O	**MII CARRIER SENSE:** This pin is asserted high when the receive medium is non-idle
24	CLK_IN	I	Reference clock from external oscillator. 25MHz ±50 ppm tolerance.

25	VDD_1P8_PLL	P	1.8V PLL power supply
26	VSS_PLL	P	PLL Ground
27	AVDD_3P3	P	3.3V analog power supply
28	RESET	I	This pin is an active high reset input that initializes or re-initializes all the internal registers.
29	MDIO	I/O	**MANAGEMENT DATA I/O**: Bidirectional command / data signal synchronized to MDC
30	MDC	I	**MANAGEMENT DATA CLOCK**: Clock signal for the management data input/output (MDIO) interface.
31	MDINT_N	O	**MANAGEMENT INTERRUPT**: if Low indicates that an interrupt condition has been detected
32	RBIAS	I	Bias Resistor Connection
33	AVSS	P	Analog Ground
34	MDI_TX_p	O	Differential transmit output (MDI mode)
35	MDI_TX_m	O	Differential transmit output (MDI mode)
36	AVDD_3P3	P	3.3V analog power supply
37	AN_speed	I	When low, it fixes the device into 10BASE-T mode. If high, the device is set to 100BASE-TX mode.
38	IOVDD_3P3	P	3.3V IO power supply
39	PWRDN_n	I	This pin is configured for a power down function, so an active low signal on this pin will put the device in power down mode.

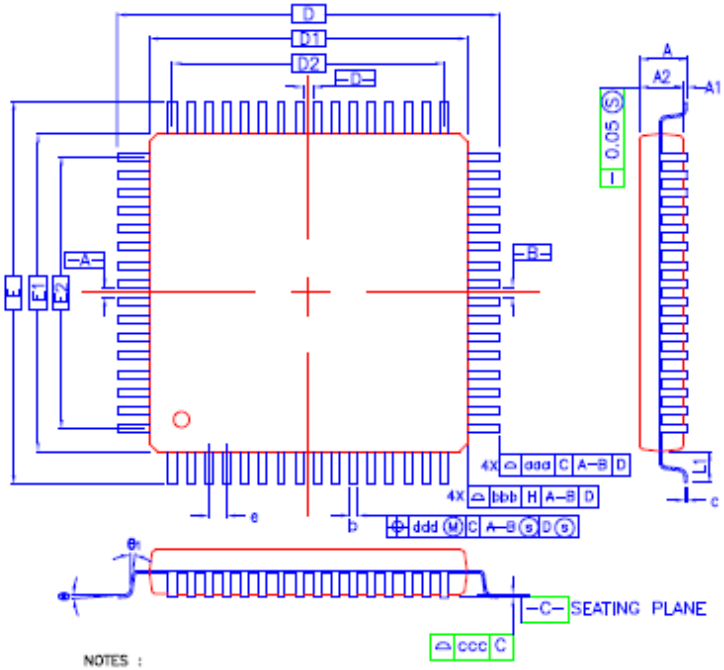
			The registers and memory will not be erased during power down mode.
40	IOVSS	P	IO Ground
41	MDI_RX_p	I	Differential transmit input (MDI mode)
42	MDI_RX_m	I	Differential transmit input (MDI mode)
43	AVSS	P	Analog Ground
44	LED_RI	O	**Receive Activity LED**. This signal is high to indicate receive activity.
45	LED _TI	O	**Transmit Activity LED.** This signal is high to indicate rec Transmit activity. It is also used as TBO_ANA_p output in test bus mode.
46	LED _LNK	O	**Link Established LED**. This signal is high to indicate the Link has been established.
47	TEST_O[0]/TBO_ANA_p	O	**Test pins** Output test pins allow generate digital signals. It is also used as TBO_ANA_p/TBO_ANA_m output in test bus mode
48	AVDD_3P3	P	3.3V analog power supply
49	TEST_O[1]/TBO_ANA_m	O	**Test pins** Output test pins allow generate digital signals. It is also used as TBO_ANA_p/TBO_ANA_M output in test bus mode.
50	TEST_I[0]/PHYADD[0]	I	**Test pins:** Input test pins allow introducing external signals, even high speed clock signals, for internal uses. **PHY Address:** These pins set the management interface physical

			address during the reset of the device. Up to 32 PHYs can be used with the same MAC layer.
51	TEST_I[1]/PHYADD[1]	I	**Test pins:** Input test pins allow introducing external signals, even high speed clock signals, for internal uses. **PHY Address:** These pins set the management interface physical address during the reset of the device. Up to 32 PHYs can be used with the same MAC layer.
52	PHYADD[2]	I	**PHY Address**. These pins set the management interface physical address of the device. Up to 32 PHYs can be used with the same MAC layer.
53	AVSS	P	Analog Ground
54	PHYADD[3]	I	**PHY Address**. These pins set the management interface physical address of the device. Up to 32 PHYs can be used with the same MAC layer.
55	AVDD_3P3	P	3.3V analog power supply
56	PHYADD[4]	I	**PHY Address**. These pins set the management interface physical address of the device. Up to 32 PHYs can be used with the same MAC layer.
57	DVSS	P	Core Ground
58	RESERVED	N/A	
59	RESERVED	N/A	
60	RESERVED	N/A	

61	DVDD_1P8	P	1.8V core power supply
62	RESERVED	N/A	
63	RESERVED	N/A	
64	IOVSS	P	IO Ground

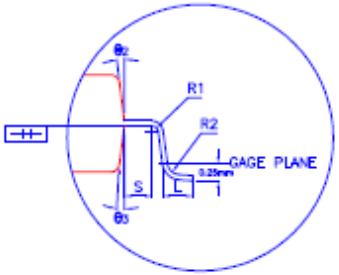
Table 10-1 SEPHY pin list

11 Package



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	64L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC.			0.031 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.20			0.008		



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

Figure 11-1: SEPHY CQF64 package

12 SUPPLY/GROUNDING LAYOUT, THERMAL RECOMMENDATIONS

12.1.1 Ground Planes

When connecting power to SEPHY chip, it is recommended that three separate supplies be used. Use one supply for the analog outputs (AVDD_3P3); a different one will be used for the I/O power supply (IOVDD_3P3). The last one will be used for the digital core (DVDD_1P8).

For better performance, two ground power planes (digital&IOs and analog) should be used and connected together in a single point below the component. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

12.1.2 Routing

Critical paths must be shielded.

Differential paths must be equalized.

12.1.3 Power decoupling

For AVDD_3P3, IOVDD_3P3 and DVDD_1P8, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length

12.1.4 Clock jitter

The clock jitter should be less than 250ps.

12.1.5 Thermal dissipation

Airflow increases heat dissipation, effectively reducing thermal resistance. Also, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the thermal resistance.

12.1.6 ESD caution

Dies are very sensitive to electrostatic discharge from other bodies or surfaces at different potentials. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. The ESD robustness of a design depends on the I/O configuration as well.